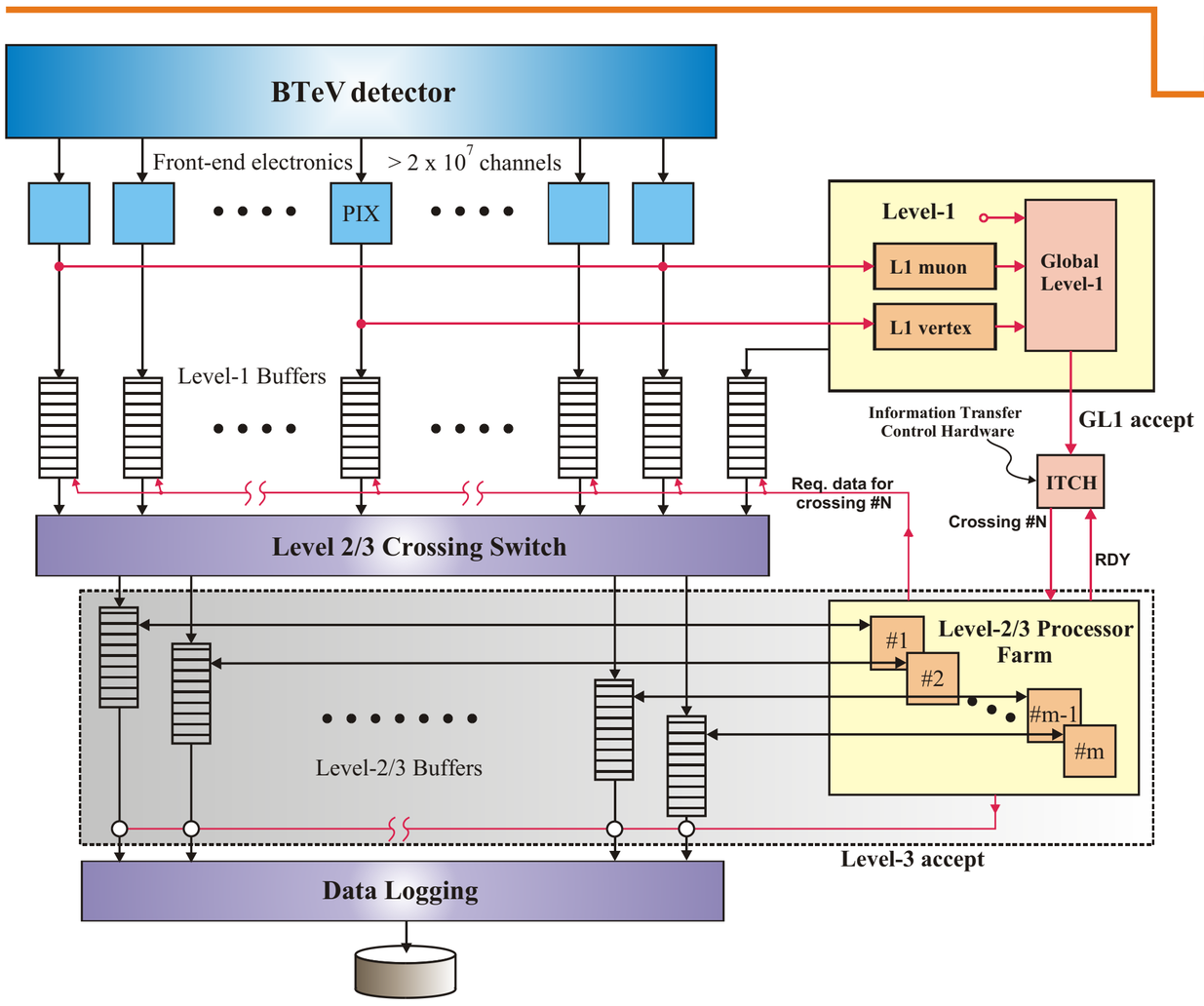
BTeV Trigger

3 Level Hierarchical Trigger



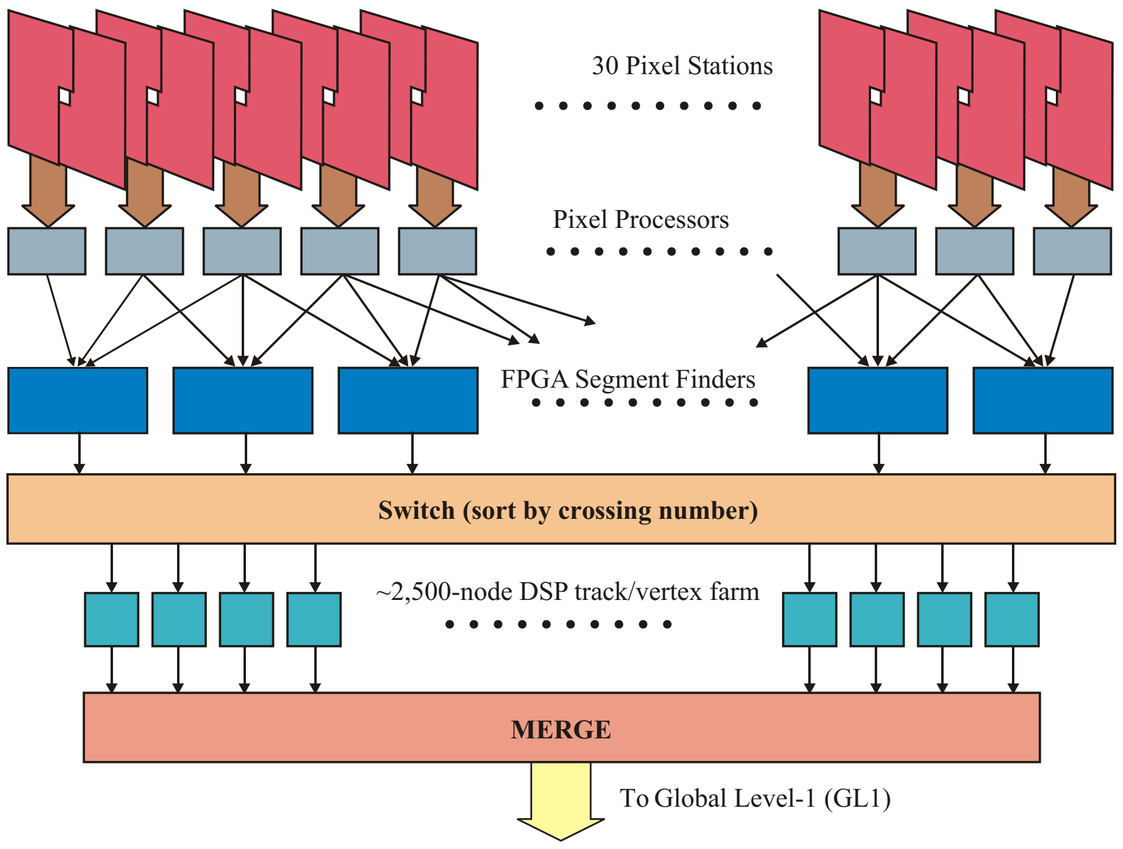
System is designed to process data at the full crossing rate of 7.6MHz (1.5TB/s) in the first level. L1 algorithm will reject 99% of all incoming events reducing data rate by ~100 to ~15 GB/s. L2 & 3 algorithms running on farm of commodity PC's will further reduce data rate by ~20. Expected data rate out of L3, after factor of ~4 data compression is ~200 MB/sec.

Level 1 Vertex Trigger

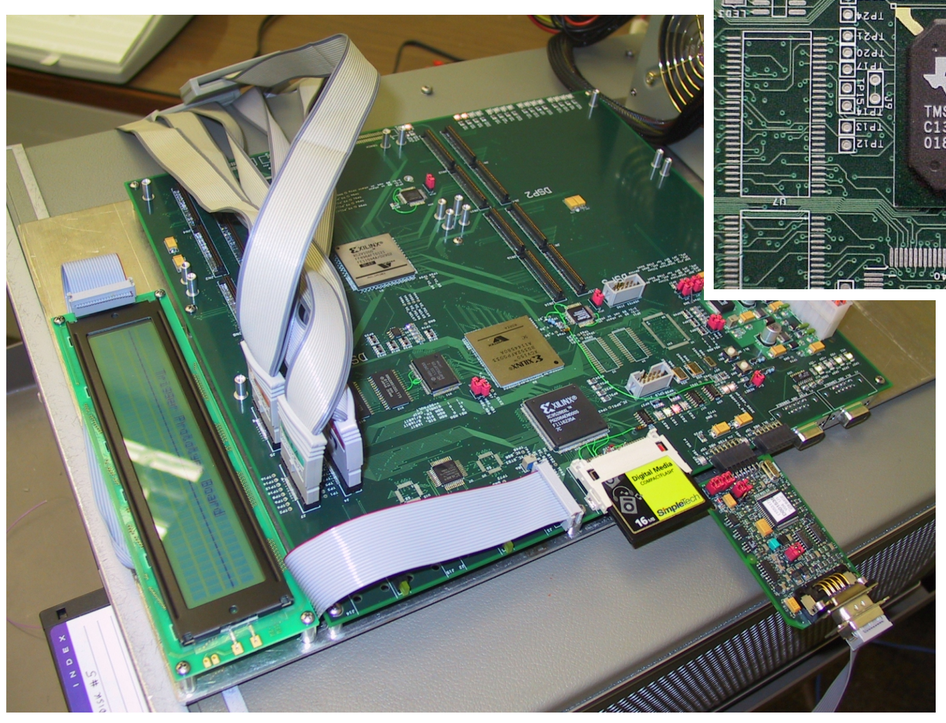
FPGA's will process data from 3 neighboring pixel stations to find beginning & ending segments of tracks (triplets). Switch will sort triplets by crossing number and send them to a processor farm* for track finding and vertexing. Trigger is generated if there are at least 2 detached tracks with:

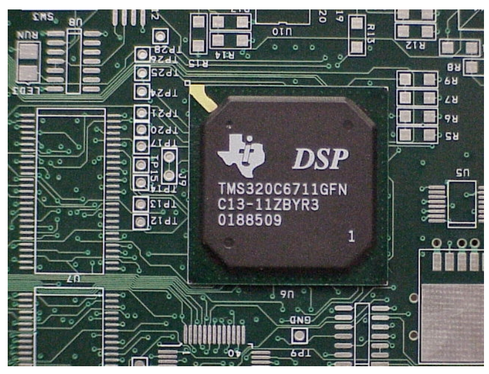
p_T^2	0.25 (GeV/c)^2
b	6
b	0.2 cm

* The L1 Muon trigger will employ a similar farm consisting of embedded processors.



4 DSP PrePrototype Board





Pre-prototype board for the L1 trigger (shown here undergoing tests) will have mezzanine sites for 4 embedded processors. High-speed LVDS transceivers will receive incoming data and send processed data. FPGA-based buffer manager will transfer data to and from embedded processors via DMA transfers. Trigger decisions will be sent to host computer via ArcNet. JTAG ports available for debugging and start-up.